MOTOROLA

MC6822

Advance Information

MOS
(N-CHANNEL, SILICON-GATE
DEPLETION LOAD)

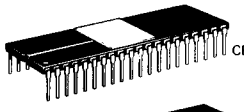
INDUSTRIAL INTERFACE ADAPTER

INDUSTRIAL INTERFACE ADAPTER (IIA)

The MC6822 Industrial Interface Adapter (IIA) provides a universal means of interfacing peripheral equipment to the M6800 Family of microprocessors. This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

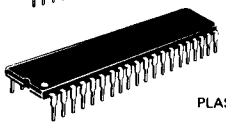
The functional configuration of the IIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or an output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines, Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- Open-Drain Port Circuits
- High Voltage Capability up to 18 Volts
- Program Controlled Interrupt and Interrupt Disable Capability
- Ports Output Compatible with CMOS at 15 Volts
- TTL Compatible
- Static Operation
- Pin Compatible with MC6821 PIA



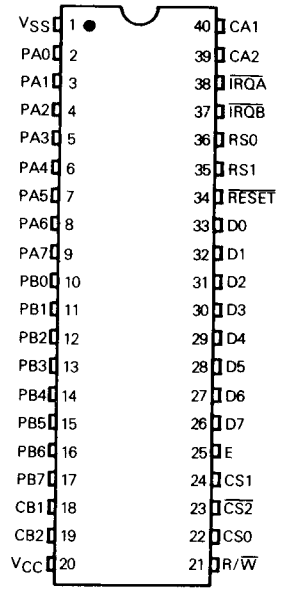
L SUFFIX
CERAMIC PACKAGE
CASE 715

S SUFFIX
CERDIP PACKAGE
CASE 734



P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN ASSIGNMENT



ORDERING INFORMATION

Package Type	Frequency	Operating Temperature	Part Number
Ceramic L Suffix	1.0 MHz	0°C to 70°C	MC6822L
	1.0 MHz	−40°C to 85°C	MC6822CL
	1.5 MHz	0°C to 70°C	MC68A22L
	1.5 MHz	−40°C to 85°C	MC68A22CL
	2.0 MHz	0°C to 70°C	MC68B22L
	2.0 MHz	−40°C to 85°C	MC68B22CL
Cerdip S Suffix	1.0 MHz	0°C to 70°C	MC6822S
	1.0 MHz	−40°C to 85°C	MC6822CS
	1.5 MHz	0°C to 70°C	MC68A22S
	1.5 MHz	−40°C to 85°C	MC68A22CS
	2.0 MHz	0°C to 70°C	MC68B22S
	2.0 MHz	−40°C to 85°C	MC68B22CS
Plastic P Suffix	1.0 MHz	0°C to 70°C	MC6822P
	1.0 MHz	−40°C to 85°C	MC6822CP
	1.5 MHz	0°C to 70°C	MC68A22P
	1.5 MHz	−40°C to 85°C	MC68A22CP
	2.0 MHz	0°C to 70°C	MC68B22P
	2.0 MHz	−40°C to 85°C	MC68B22CP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 7.0	V
Input Voltage PA0-PA7, CA1, CA2, PB0-PB7, CB1, CB2 All Others	V_{in}	−0.3 to 18.0 −0.3 to 7.0	V
Operating Temperature Range MC6822, MC68A22, MC68B22 MC6822C, MC68A22C, MC68B22C	T_A	T_L to T_H 0 to 70 −40 to 85	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage (i.e., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Ceramic Plastic Cerdip	θ_{JA}	 50 100 60	°C/W

3

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

$T_A \equiv$ Ambient Temperature, °C

$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{PORT} \equiv$ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

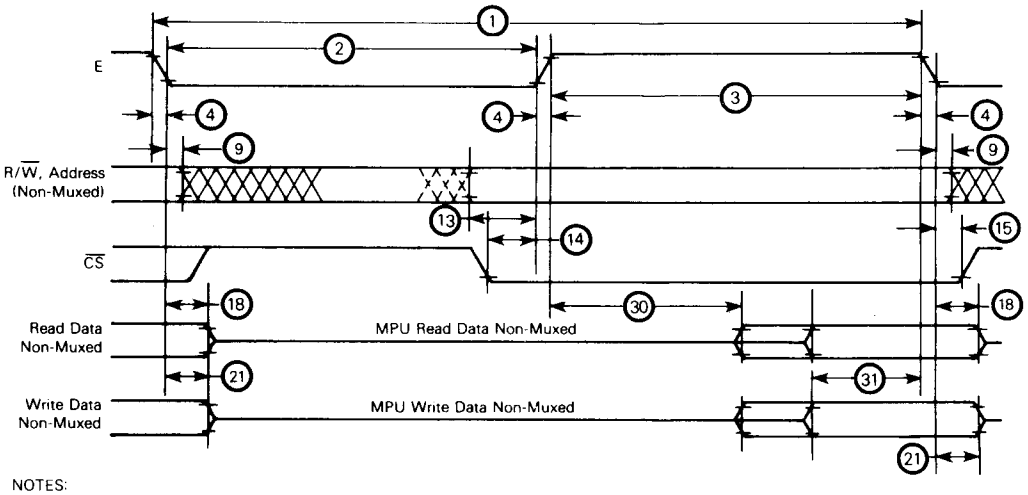
DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, $T_A = T_L$ to T_H, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BUS CONTROL INPUTS (R/$\overline{W}$, Enable, $\overline{RESET}$, RS0, RS1, CS0, CS1, $\overline{CS2}$)					
Input High Voltage	V_{IH}	V_{SS} + 2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS} − 0.3	–	V_{SS} + 0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)	I_{in}	–	1.0	2.5	μA
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{in}	–	–	7.5	pF
INTERRUPT OUTPUTS ($\overline{IRQA}$, $\overline{IRQB}$)					
Output Low Voltage (I_{Load} = 1.6 mA)	V_{OL}	–	–	V_{SS} + 0.4	V
Hi-Z Output Leakage Current	I_{OZ}	–	1.0	10	μA
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	–	–	5.0	pF
DATA BUS (D0-D7)					
Input High Voltage	V_{IH}	V_{SS} + 2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS} − 0.3	–	V_{SS} + 0.8	V
Hi-Z Input Leakage Current (V_{in} = 0.4 to 2.4 V)	I_{IZ}	–	2.0	10	μA
Output High Voltage (I_{Load} = 205 μA)	V_{OH}	V_{SS} + 2.4	–	–	V
Output Low Voltage (I_{Load} = 1.6 mA)	V_{OL}	–	–	V_{SS} + 0.4	V
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{in}	–	–	12.5	pF
PERIPHERAL BUS (PA0-PA7, PB0-PB7, CA1, CA2, CB1, CB2)					
Port Leakage High Current (V_{in} = 16 V)	I_{PLKH}	–	–	10	μA
Port Leakage Low Current (V_{in} = 10 V)	I_{PLKL}	–	–	2.5	μA
Output Low Voltage (I_{Load} = 1 mA)	V_{OL}	–	–	0.4	V
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{in}	–	–	10	pF
POWER REQUIREMENTS					
Internal Power Dissipation (Measured at $T_A = T_L$)	P_{INT}	–	–	550	mW

BUS TIMING CHARACTERISTICS (See Notes 1 and 2)

Ident. Number	Characteristic	Symbol	MC6822		MC68A22		MC68B22		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	μs
2	Pulse Width, E Low	PW_{EL}	430	–	280	–	210	–	ns
3	Pulse Width, E High	PW_{EH}	450	–	280	–	220	–	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	20	ns
9	Address Hold Time	t_{AH}	10	–	10	–	10	–	ns
13	Address Setup Time Before E	t_{AS}	80	–	60	–	40	–	ns
14	Chip Select Setup Time Before E	t_{CS}	80	–	60	–	40	–	ns
15	Chip Select Hold Time	t_{CH}	10	–	10	–	10	–	ns
18	Read Data Hold Time	t_{DHR}	20	–	20	–	20	–	ns
21	Write Data Hold Time	t_{DHW}	10	–	10	–	10	–	ns
30	Output Data Delay Time	t_{DDR}	–	290	–	180	–	150	ns
31	Input Data Setup Time	t_{DSW}	165	–	80	–	60	–	ns

BUS TIMING



NOTES:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

PERIPHERAL TIMING CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0 V, $T_A = T_L$ to T_H, unless otherwise noted)

Characteristic	Symbol	MC6822		MC68A22		MC68B22		Unit	Reference Fig. No.
		Min	Max	Min	Max	Min	Max		
Data Setup Time	t_{PDS}	200	–	135	–	100	–	ns	4
Data Hold Time	t_{PDH}	0	–	0	–	0	–	ns	4
Delay Time, Enable Negative Transition to CA2 Negative Transition	t_{CA2}	–	1.0	–	0.670	–	0.500	µs	1, 5, 6
Delay Time, Enable Negative Transition to CA2 Positive Transition	t_{RS1}	–	1.0	–	0.670	–	0.500	µs	1, 5
Rise and Fall Times for CA1 and CA2 Input Signals	t_r, t_f	–	1.0	–	1.0	–	1.0	µs	6
Delay Time from CA1 Active Transition to CA2 Postive Transition	t_{RS2}	–	2.0	–	1.35	–	1.0	µs	1, 6
Delay Time, Enable Negative Transition to Data Valid	t_{PDW}	–	1.0	–	0.670	–	0.5	µs	1, 7, 8
Delay Time, Enable Positive Transition to CB2 Negative Transition	t_{CB2}	–	1.0	–	0.670	–	0.5	µs	1, 9, 10
Delay Time, Data Valid to CB2 Negative Transition	t_{DC}	20	–	20	–	20	–	ns	1, 8
Delay Time, Enable Positive Transition to CB2 Positive Transition	t_{RS1}	–	1.0	–	0.670	–	0.5	µs	1, 9
Control Output Pulse Width, CA2/CB2	PW_{CT}	550	–	200	–	50	–	ns	1, 9
Rise and Fall Time for CB1 and CB2 Input Signals	t_r, t_f	–	1.0	–	1.0	–	1.0	µs	10
Delay Time, CB1 Active Transition to CB2 Positive Transition	t_{RS2}	–	2.0	–	1.35	–	1.0	µs	1, 10
Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$	t_{IR}	–	1.60	–	1.10	–	0.85	µs	3, 12
Interrupt Response Time	t_{RS3}	–	1.0	–	0.8	–	0.6	µs	3, 11
Interrupt Input Pulse Time	PW_I	500	–	330	–	250	–	ns	11
$\overline{RESET}$ Low Time*	t_{RL}	1.0	–	0.66	–	0.5	–	µs	13

* The $\overline{RESET}$ line must be high a minimum of 1.0 µs before addressing the IIA.

FIGURE 1 — BUS TIMING TEST LOADS

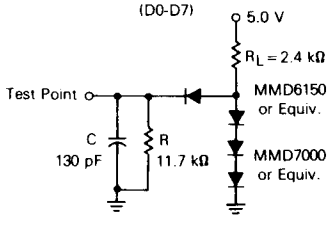
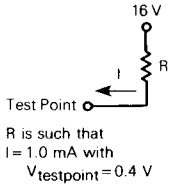


FIGURE 2 — TEST LOADS FOR PA0-PA7, PB0-PB7, CA2, CB2



R is such that
I = 1.0 mA with
$V_{testpoint}$ = 0.4 V

FIGURE 3 — NMOS EQUIVALENT TEST LOAD

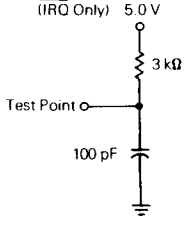
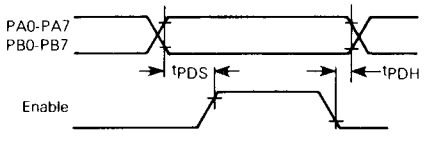
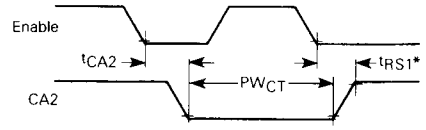


FIGURE 4 — PERIPHERAL DATA SETUP AND HOLD TIMES (READ MODE)



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts unless otherwise noted.

FIGURE 5 — CA2 DELAY TIME
(READ MODE: CRA-5 = CRA-3 = 1,
CRA-4 = 0)



*Assumes part was deselected during the previous E pulse.

FIGURE 6 — CA2 DELAY TIME
(READ MODE: CRA-5 = 1,
CRA-3 = CRA-4 = 0)

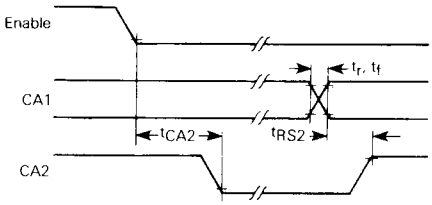


FIGURE 7 — PERIPHERAL CMOS DATA
DELAY TIMES
(WRITE MODE: CRA-5 = CRA-3 = 1,
CRA-4 = 0)

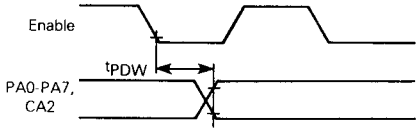
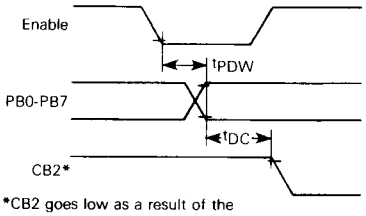
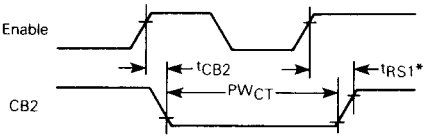


FIGURE 8 — PERIPHERAL DATA AND
CB2 DELAY TIMES
(WRITE MODE: CRB-5 = CRB-3 = 1,
CRB-4 = 0)



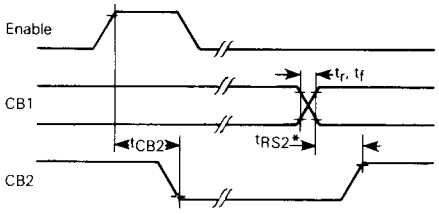
*CB2 goes low as a result of the positive transition of enable.

FIGURE 9 — CB2 DELAY TIME
(WRITE MODE: CRB-5 = CRB-3 = 1,
CRB-4 = 0)



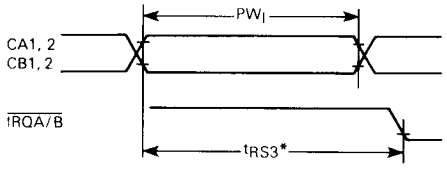
*Assumes part was deselected during the previous E pulse.

FIGURE 10 — CB2 DELAY TIME
(WRITE MODE: CRB-5 = 1,
CRB-3 = CRB-4 = 0)



*Assumes part was deselected during any previous E pulse.

FIGURE 11 — INTERRUPT PULSE WIDTH
AND $\overline{IRQ}$ RESPONSE



*Assumes interrupt enable bits are set.

FIGURE 12 — $\overline{IRQ}$ RELEASE TIME

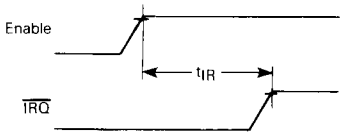
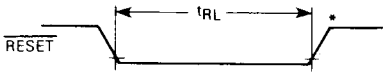


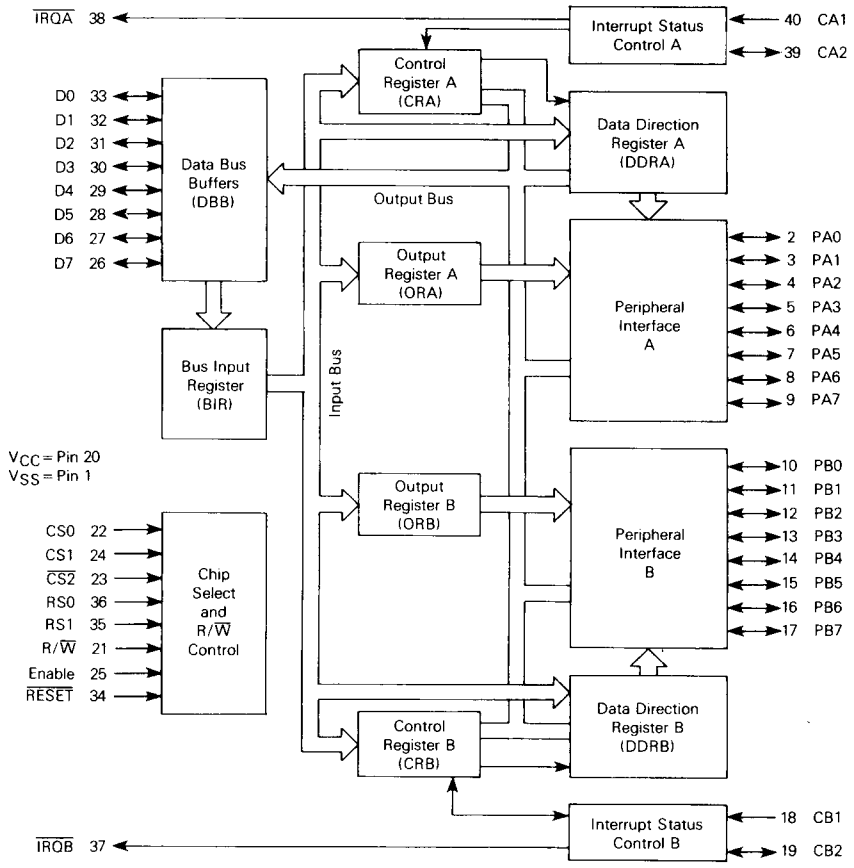
FIGURE 13 — $\overline{RESET}$ LOW TIME



*The $\overline{RESET}$ line must be a V_{IH} for a minimum of 1.0 μs before addressing the IIA.

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 14 — EXPANDED BLOCK DIAGRAM



IIA INTERFACE SIGNALS FOR MPU

The IIA interfaces to the M6800 bus with an 8-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, a read/write line, an enable line, and a reset line. To ensure proper operation with the MC6800, MC6802, or MC6808 microprocessors, VMA should be used as an active part of the address decoding.

BIDIRECTIONAL DATA (D0-D7)

The bidirectional data lines (D0-D7) allow the transfer of data between the MPU and the IIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an IIA read operation. The read/write line is in the read (high) state when the IIA is selected for a read operation.

ENABLE (E)

The enable pulse, E, is the only timing signal that is supplied to the IIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse.

READ/WRITE (R/$\overline{W}$)

This signal is generated by the MPU to control the direction of data transfers on the data bus. A low state on the IIA read/write line enables the input buffers and data is transferred from the MPU to the IIA on the E signal if the device has been selected. A high on the read/write line sets up the IIA for a transfer of data to the MPU data bus. The IIA output buffers are enabled when the proper address and the enable pulse, E, are present.

RESET ($\overline{RESET}$)

The active low $\overline{RESET}$ line is used to reset all register bits in the IIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.

CHIP SELECTS (CS0, CS1, AND $\overline{CS2}$)

These three input signals are used to select the IIA. CS0 and CS1 must be high and $\overline{CS2}$ must be low for selection of the device. Data transfers are then performed under the control of the enable and read/write signals. The chip-select lines must be stable for the duration of the E pulse. The device is deselected when any of the chip selects are in the inactive state.

REGISTER SELECTS (RS0 AND RS1)

The two register select lines are used to select the various registers inside the IIA. These two lines are used in conjunction with internal control registers to select a particular register that is to be written or read.

The register and chip-select lines should be stable for the duration of the E pulse while in the read or write cycle.

INTERRUPT REQUEST ($\overline{IRQA}$ AND $\overline{IRQB}$)

The active low interrupt request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open drain" (no load device on the chip). This permits all interrupt request lines to be tied together in a wire-OR configuration.

Each interrupt request line has two internal interrupt flag bits that can cause the interrupt request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also, four interrupt enable bits are provided in the IIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU may be accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each IIA for interrupt flag bits that are set.

The interrupt flags are cleared (zeroed) as a result of an MPU read peripheral data operation of the corresponding data register. After being cleared, the interrupt flag bit cannot be enabled to be set until the IIA is deselected during an E pulse. The E pulse is used to condition the interrupt control lines (CA1, CA2, CB1, CB2). When these lines are used as interrupt inputs, at least one E pulse must occur from the inactive edge to the active edge of the interrupt input signal to condition the edge sense network. If the interrupt flag has been enabled and the edge sense circuit has been properly conditioned, the interrupt flag will be set on the next active transition of the interrupt input pin.

IIA PERIPHERAL INTERFACE LINES

The IIA provides two 8-bit bidirectional data buses and four interrupt control lines for interfacing to peripheral devices.

SECTION A PERIPHERAL DATA (PA0-PA7)

Each of the peripheral data lines can be programmed to act as an input or an open-drain output. This is accomplished by setting a one in the corresponding data direction register bit for those lines which are to be outputs. A zero in a bit of the data direction register causes the corresponding peripheral data line to act as an input. During an MPU read peripheral data operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU data bus lines.

The data in output register A will appear on the data lines that are programmed to be outputs. A logical one written into the register will cause the corresponding data line to go into a high-impedance state, and may be pulled up externally to a maximum of 18 volts. A logical zero written into the register results in a low on the corresponding data line. Data in output register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic one output and less than 0.8 volts for a logic zero output.

SECTION B PERIPHERAL DATA (PB0-PB7)

The peripheral data lines in the B section of the IIA can be programmed to act as either inputs or outputs in a manner similar to PA0-PA7. Data on the peripheral data lines PB0-PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a "high" or above 0.8 volts for a "low."

INTERRUPT INPUT (CA1 AND CB1)

Peripheral input lines CA1 and CB1 are input-only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.

PERIPHERAL CONTROL (CA2)

The peripheral control line CA2 can be programmed to act as an interrupt input or as an open-drain output. The function of this signal line is programmed with control register A.

PERIPHERAL CONTROL (CB2)

Peripheral control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. This line is programmed by control register B.

INTERNAL CONTROLS

INITIALIZATION

A $\overline{RESET}$ has the effect of zeroing all IIA registers. This will set PA0-PA7, PB0-PB7, CA2, and CB2 as inputs, and disable all interrupts. The IIA must be configured during the restart program which follows the reset.

There are six locations within the IIA accessible to the MPU data bus: two peripheral registers, two data direction registers, and two control registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the control registers, as shown in Table 1.

TABLE 1 — INTERNAL ADDRESSING

Control Register Bit				
RS1	RS0	CRA-2	CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

Details of possible configurations of the data direction and control register are given in the following paragraphs.

3

PORT A-B HARDWARE CHARACTERISTICS

As shown in Figure 15, the MC6822 has a pair of I/O ports whose characteristics differ slightly.

Notice the differences between a port A and port B read operation when in the output mode. When reading port A, the actual pin is read, whereas the B side read comes from an output latch, ahead of the actual pin.

CONTROL REGISTERS (CRA AND CRB)

The two control registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1, and CB2. In addition, they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1, or CB2. The format of the control words is shown in Figure 16.

DATA DIRECTION ACCESS CONTROL BIT (CRA-2 AND CRB-2)

Bit 2 of each control register (CRA and CRB) determines selection of either a peripheral output register or the corresponding data direction registers when the proper register select signals are applied to RS0 and RS1. A one in bit 2 allows access of the peripheral data register, while a zero causes the data direction register to be addressed.

CONTROL OF CA2 AND CB2 PERIPHERAL CONTROL LINES (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, AND CRB-5)

Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 peripheral control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different loading characteristics.

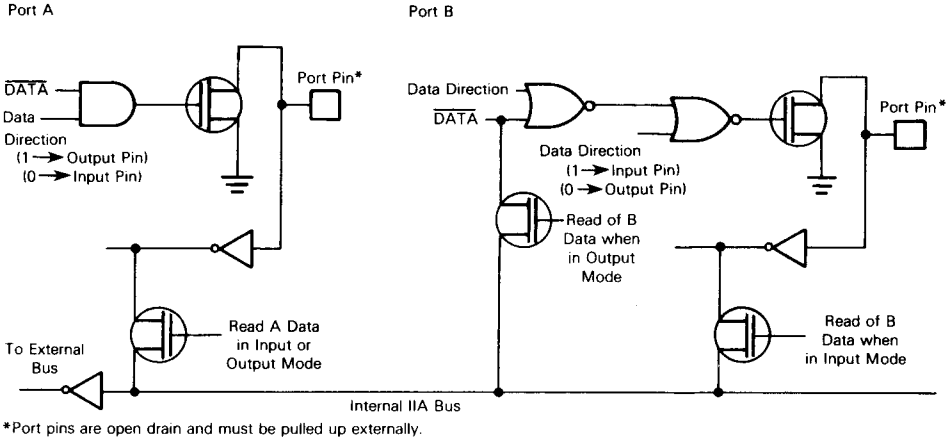
CONTROL OF CA1 AND CB1 INTERRUPT INPUT LINES (CRA-0, CRA-1, CRB-0, AND CRB-1)

The two lowest-order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1.

INTERRUPT FLAGS (CRA-6, CRA-7, CRB-6, AND CRB-7)

The four interrupt flag bits are set by active transitions of signals on the four interrupt and peripheral control lines when those lines are programmed to be inputs. These bits cannot be set directly from the MPU data bus and are reset indirectly by a read peripheral data operation on the appropriate section.

FIGURE 15 — PORT A AND PORT B EQUIVALENT CIRCUITS



*Port pins are open drain and must be pulled up externally.

FIGURE 16 — CONTROL WORD FORMAT